

1/26

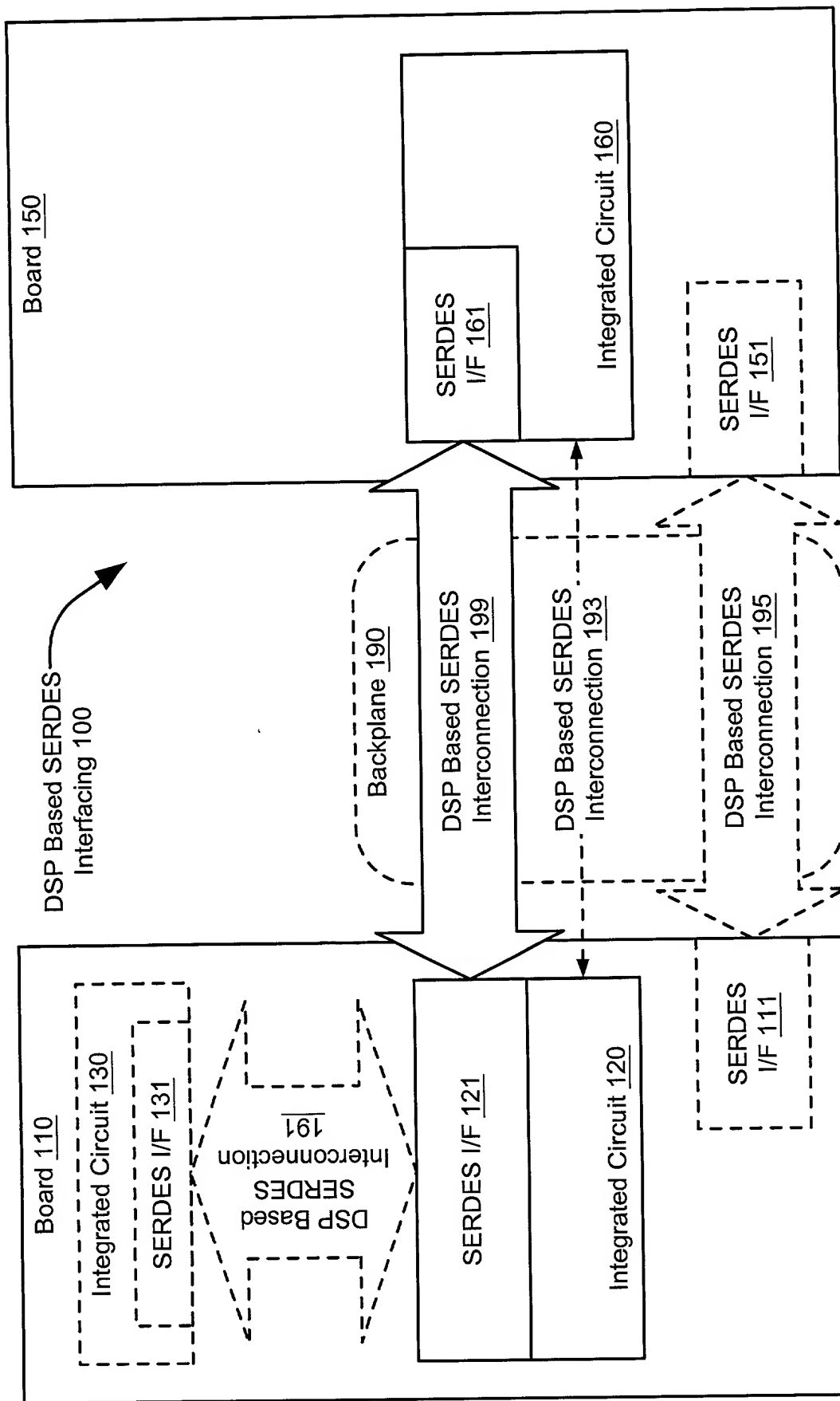


Fig. 1

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— Digital Signal Processing  
(DSP) Based SERDES  
System 200

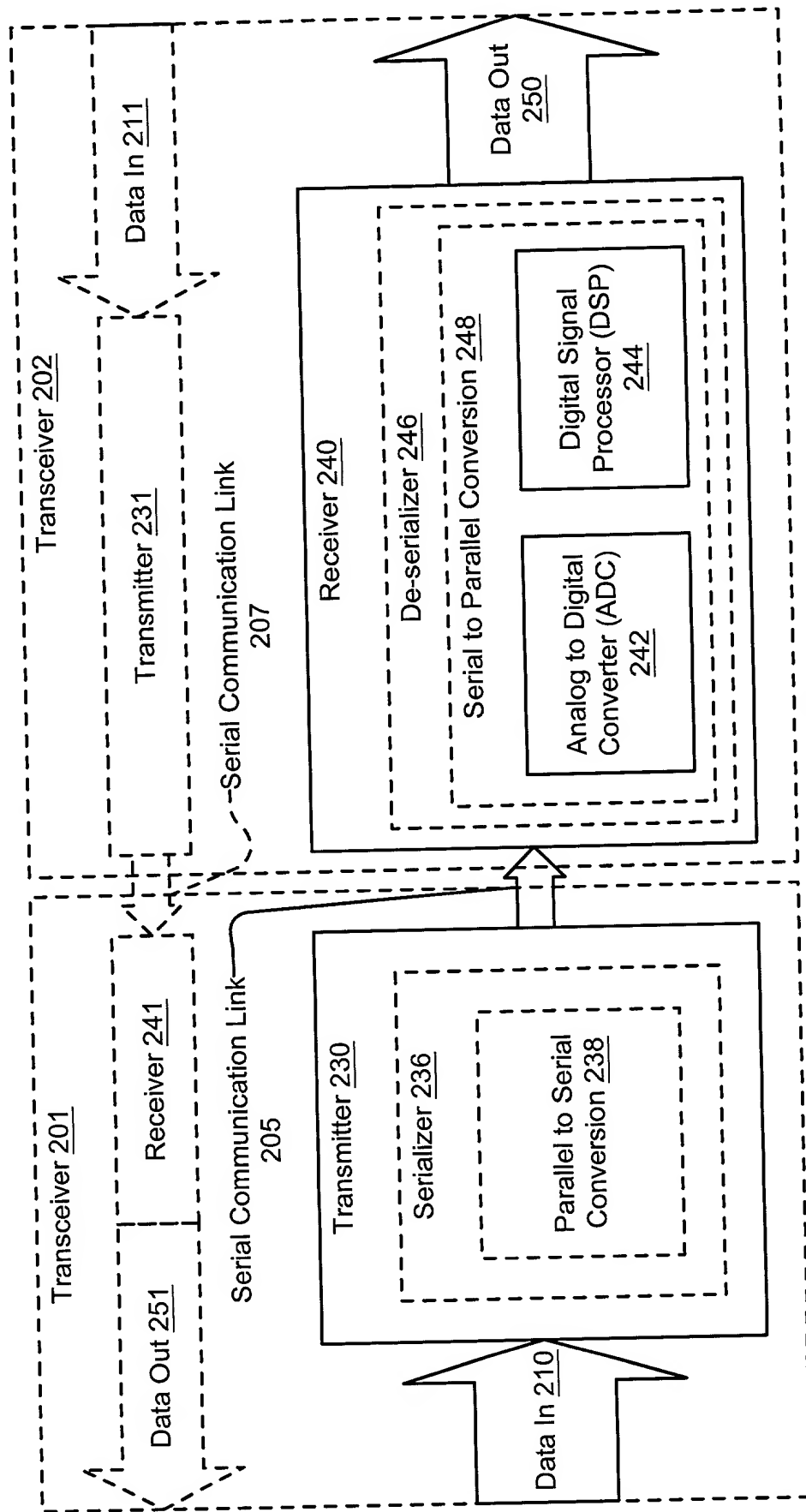


Fig. 2

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DSP Based Deserializer  
Interfacing 300

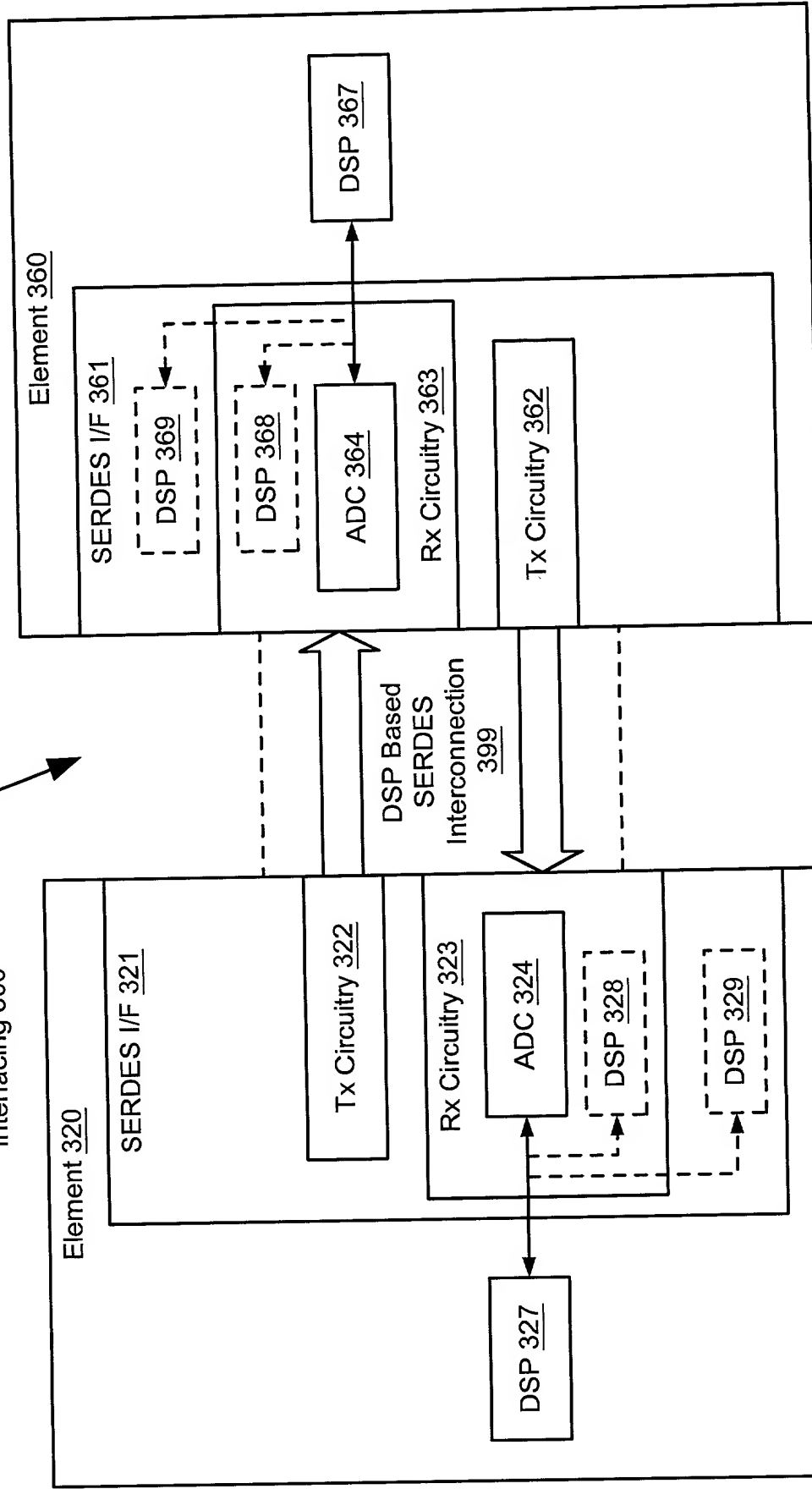


Fig. 3

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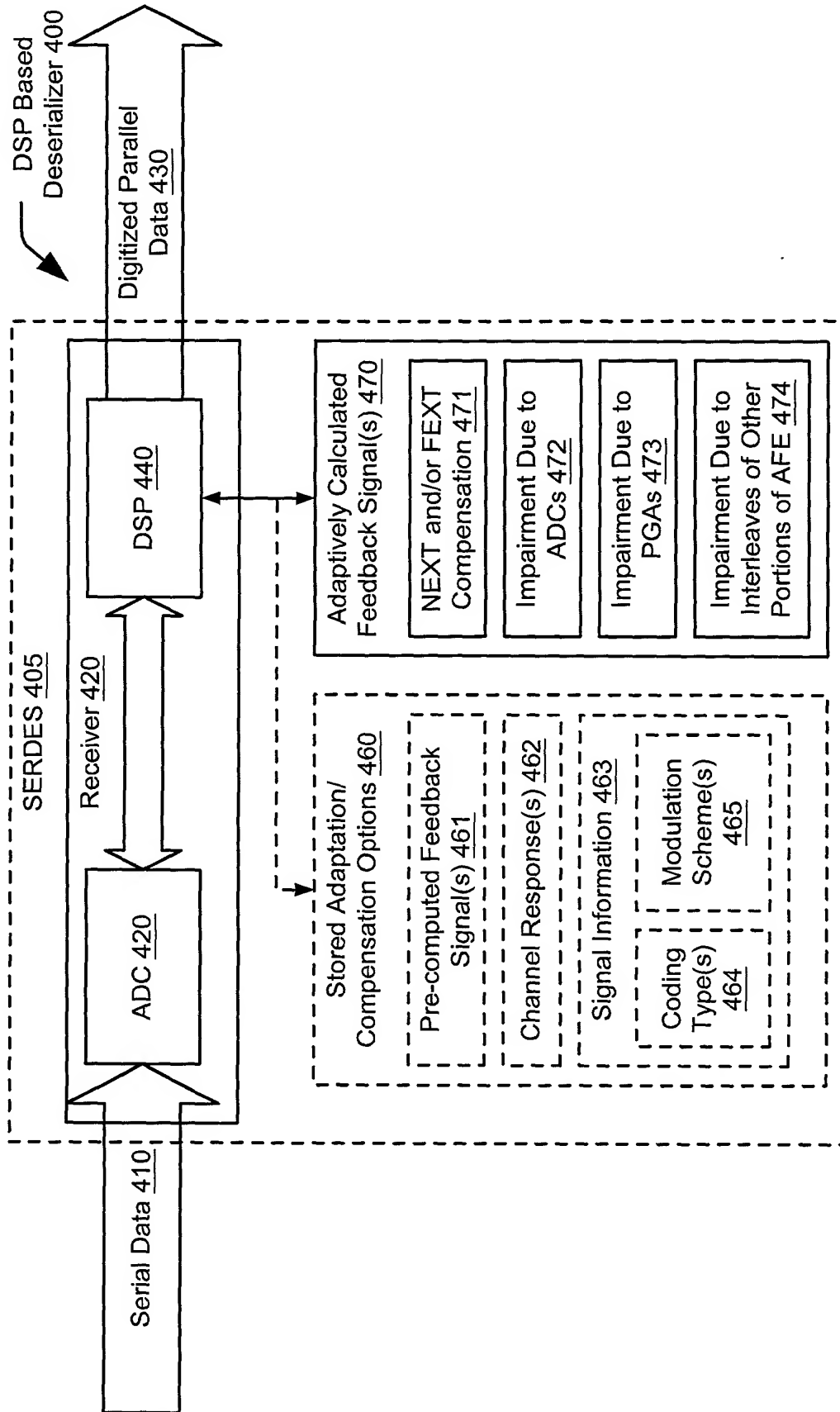


Fig. 4

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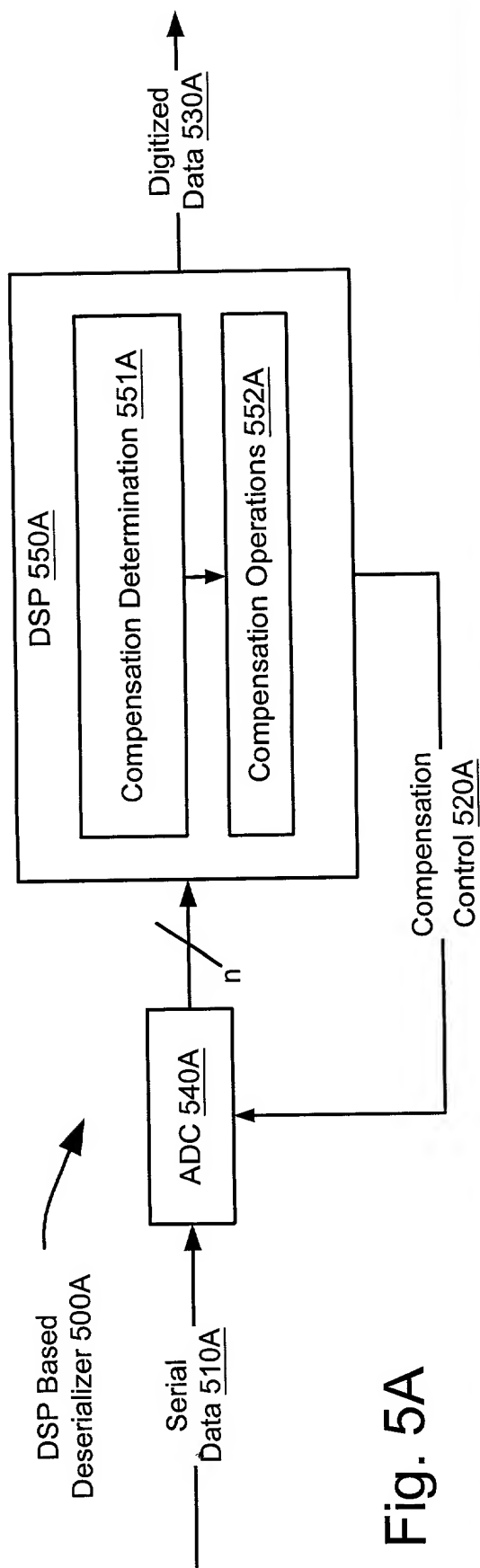


Fig. 5A

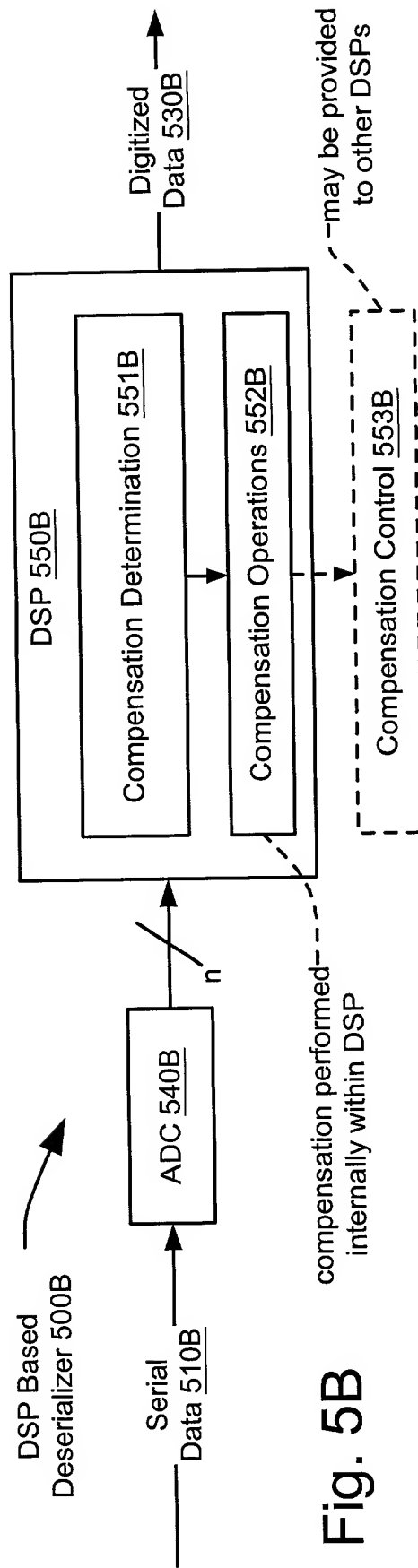


Fig. 5B

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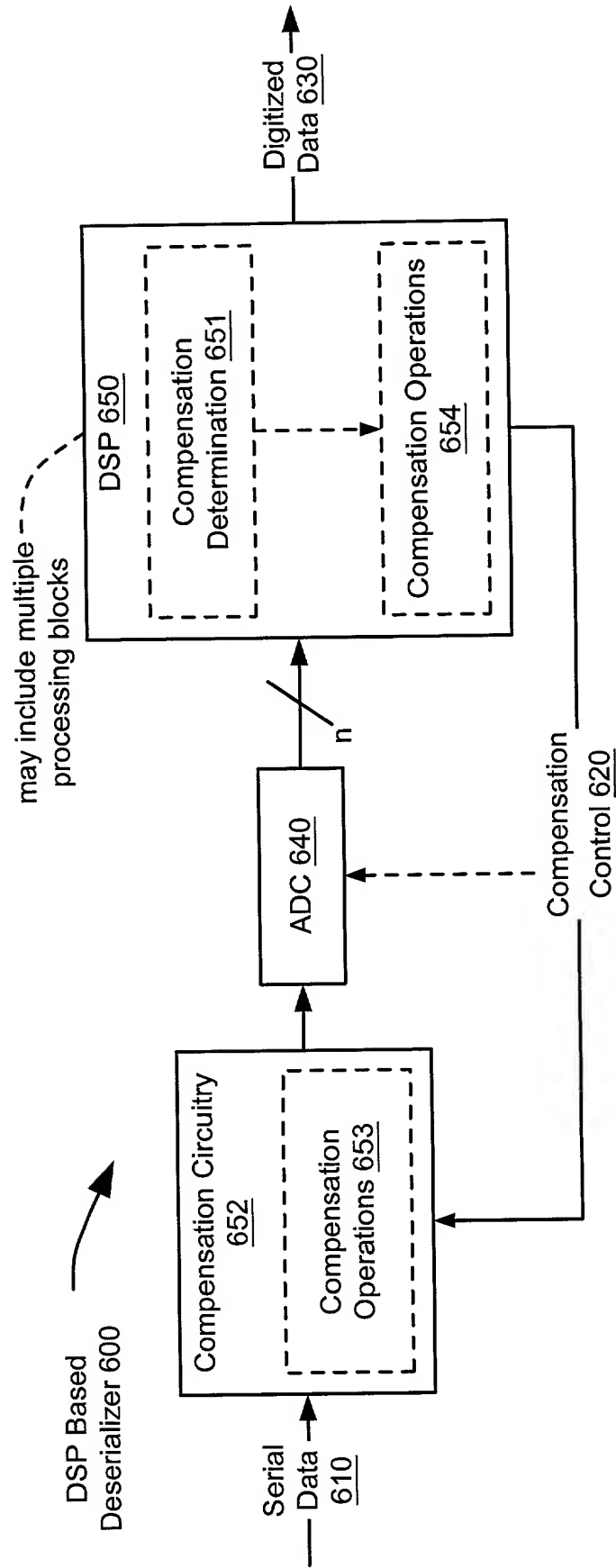


Fig. 6

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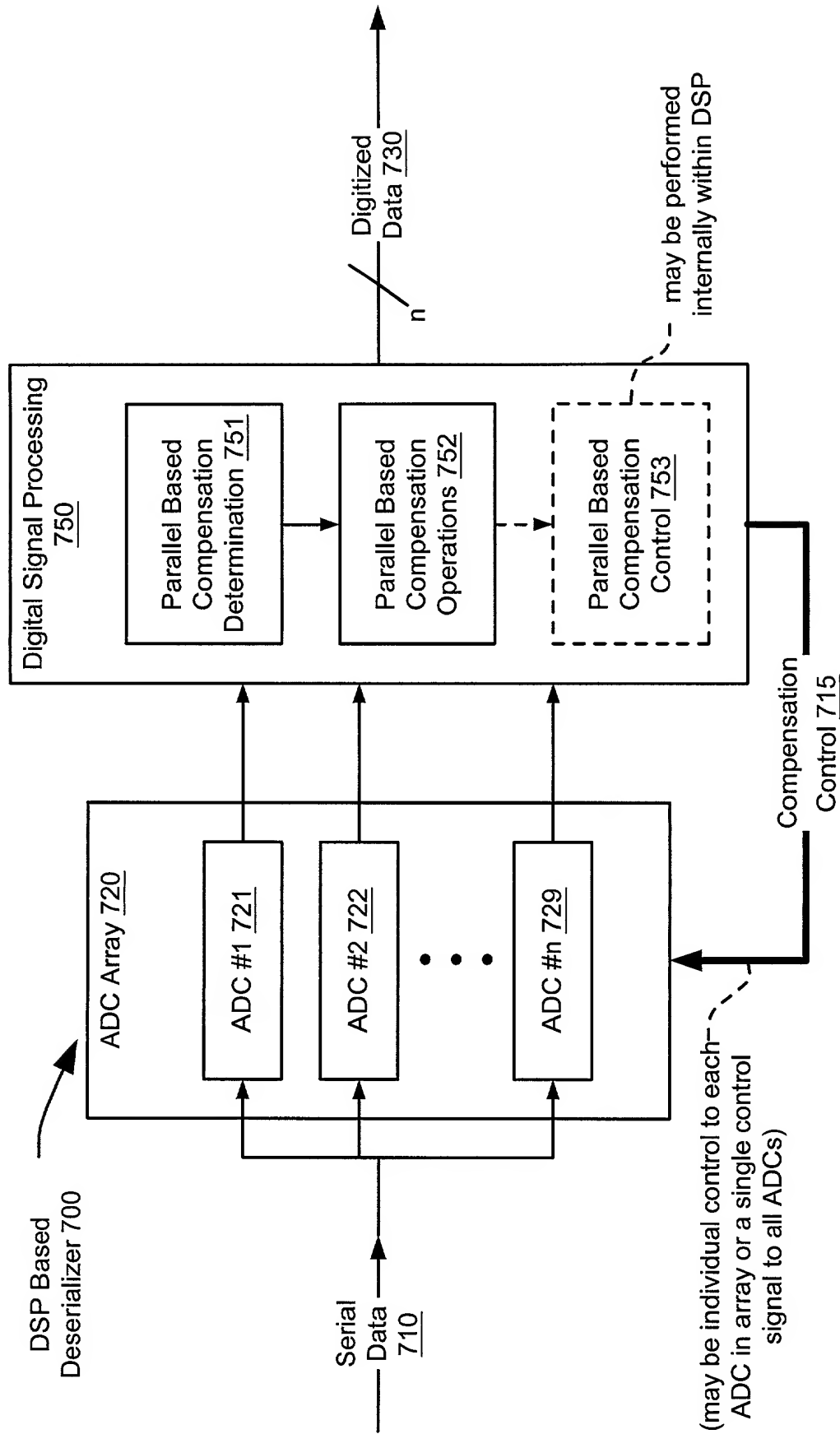


Fig. 7

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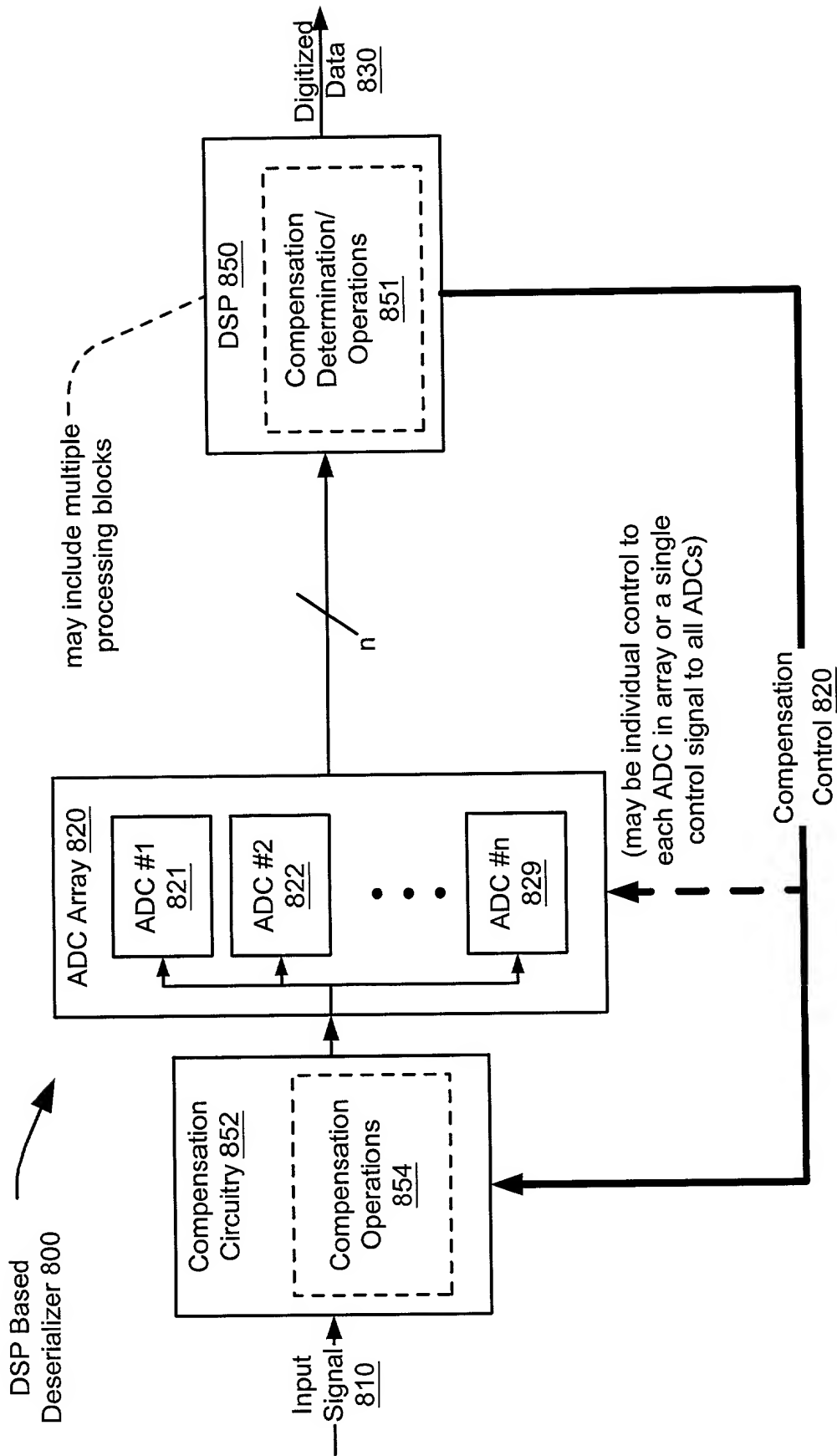


Fig. 8



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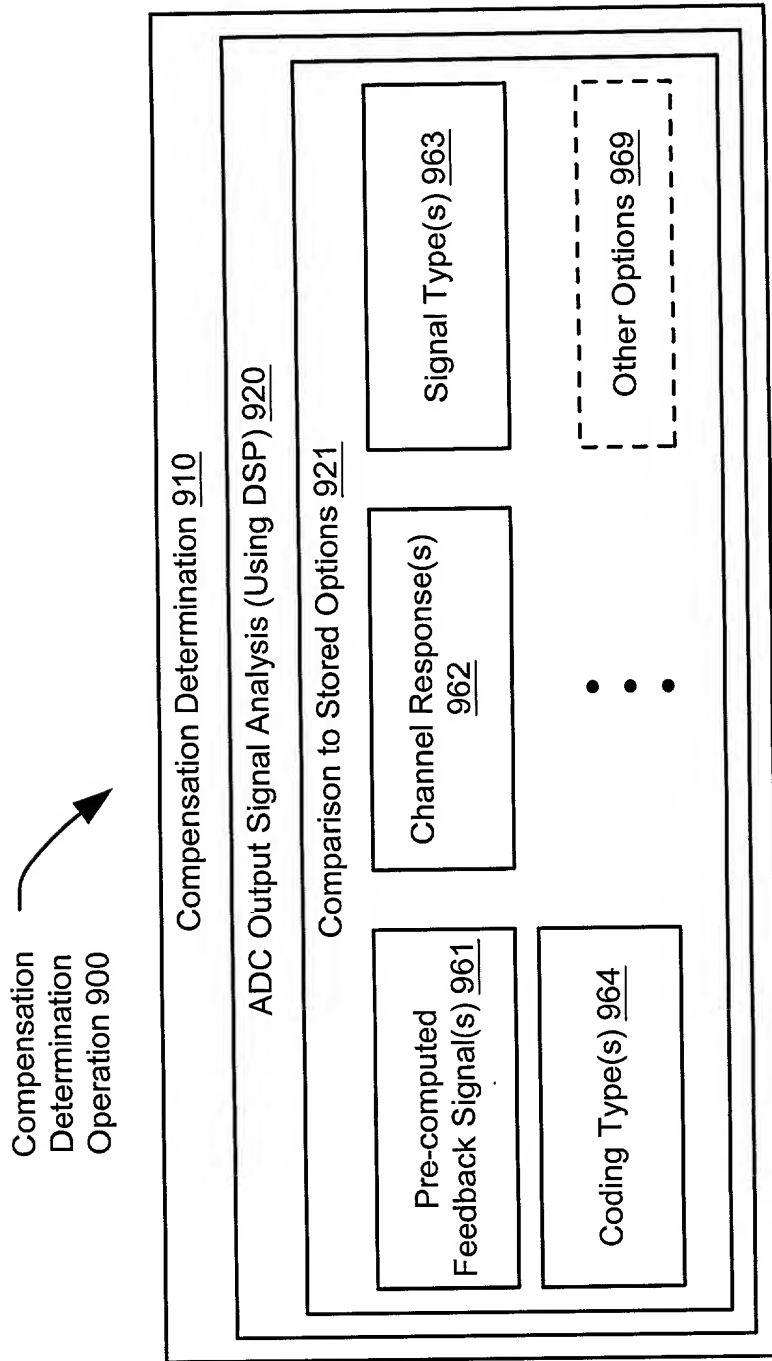


Fig. 9

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Compensation Control  
Operation 1000

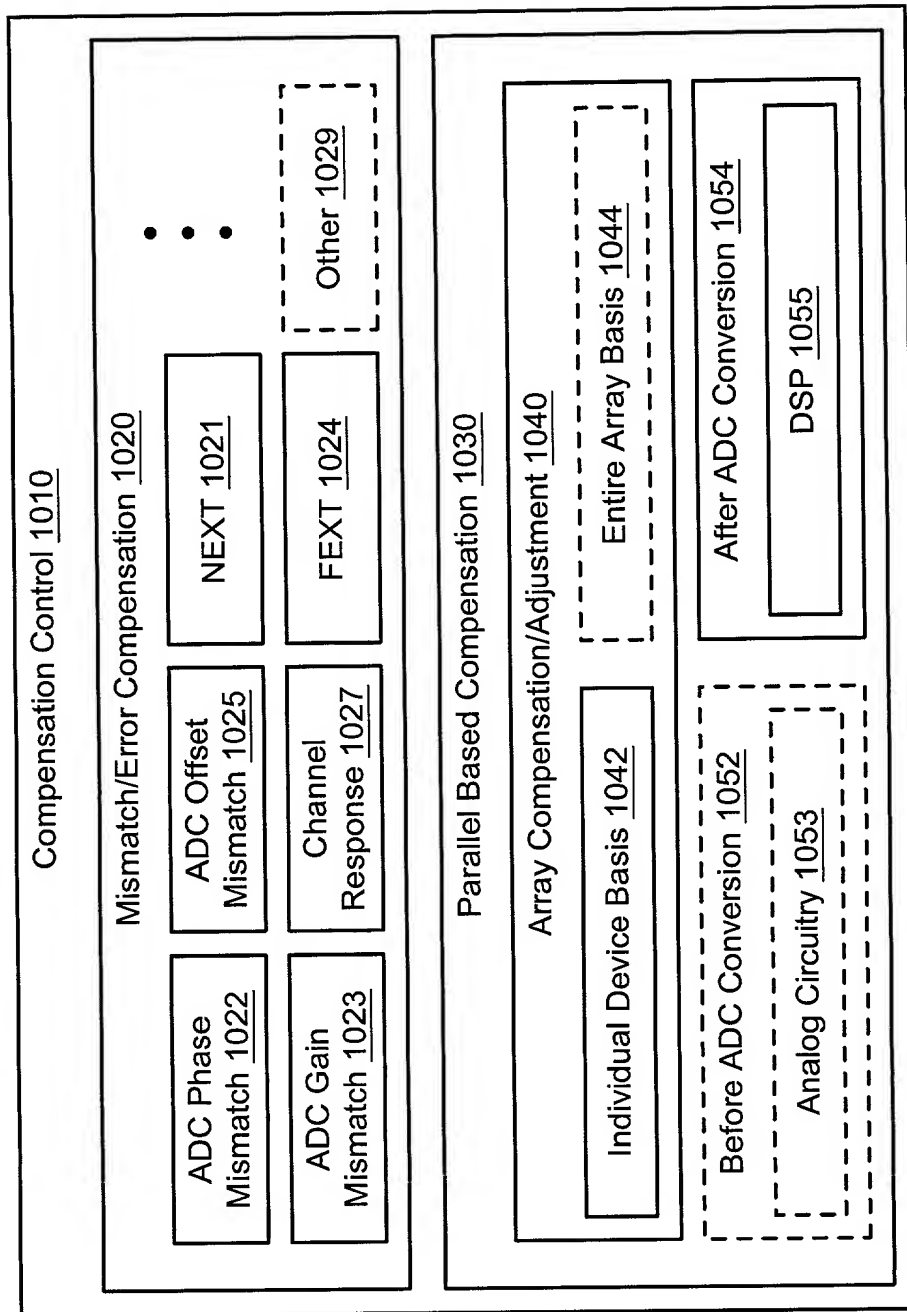


Fig. 10

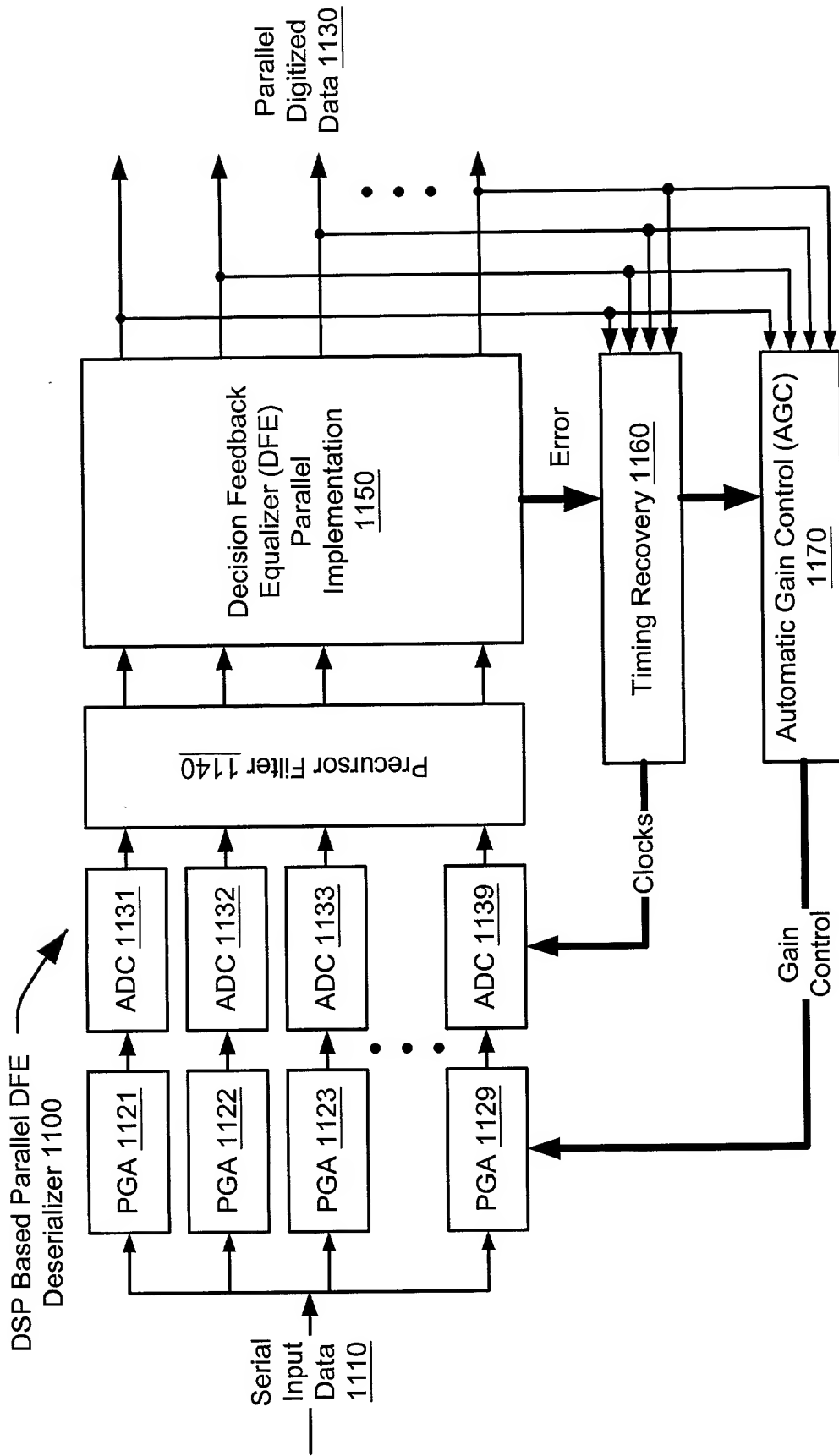


Fig. 11

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Serial to Parallel  
Implementation of  
DFE 1200

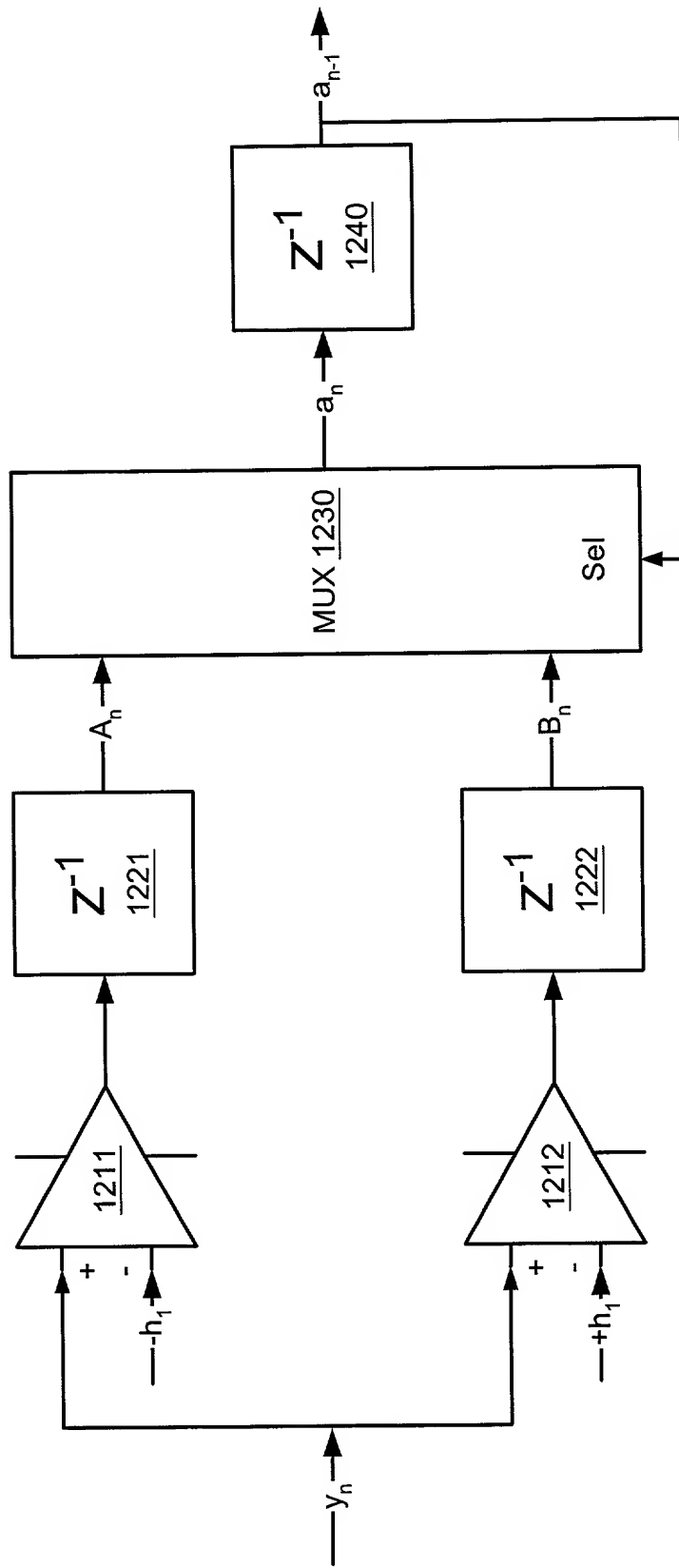


Fig. 12

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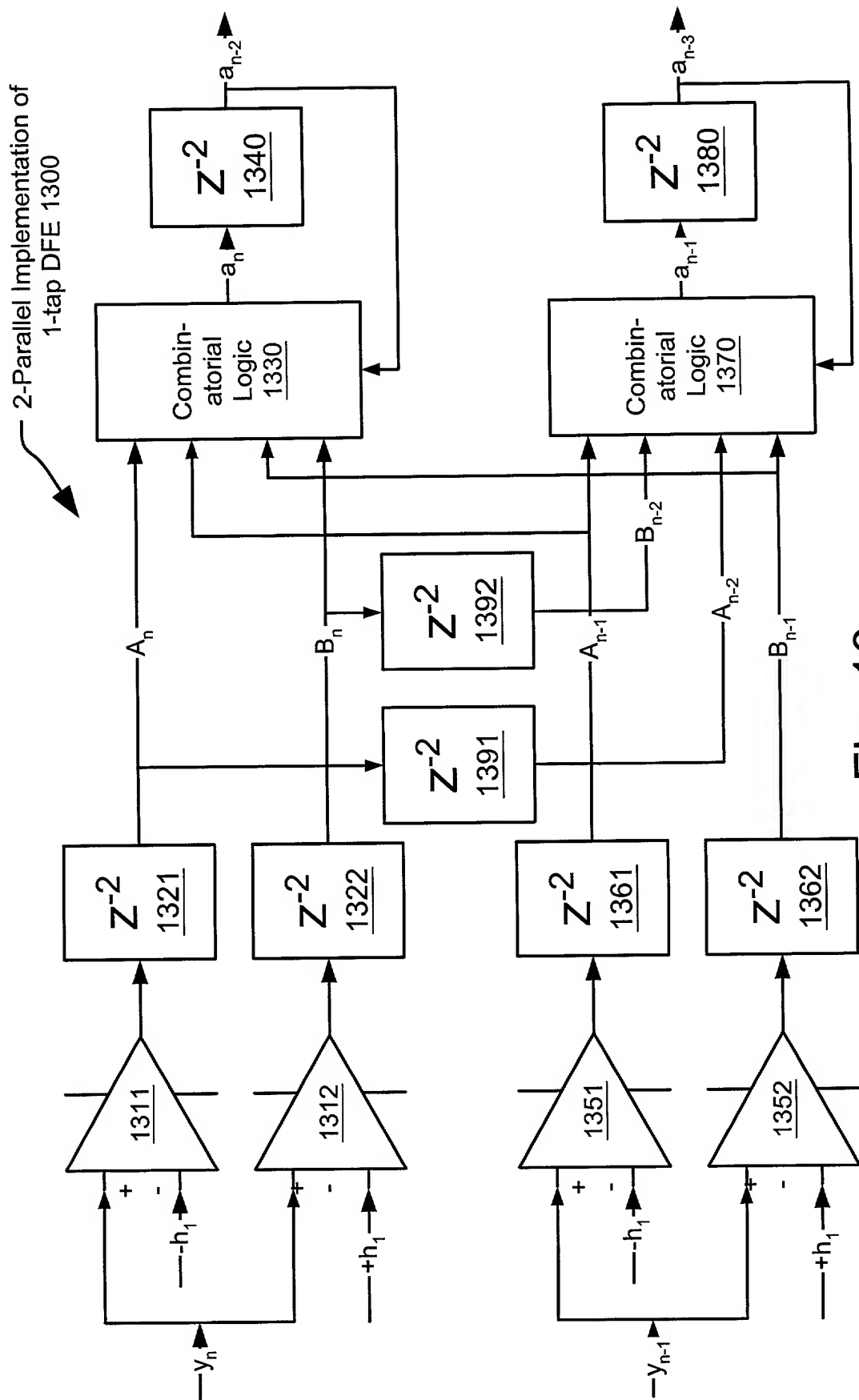


Fig. 13

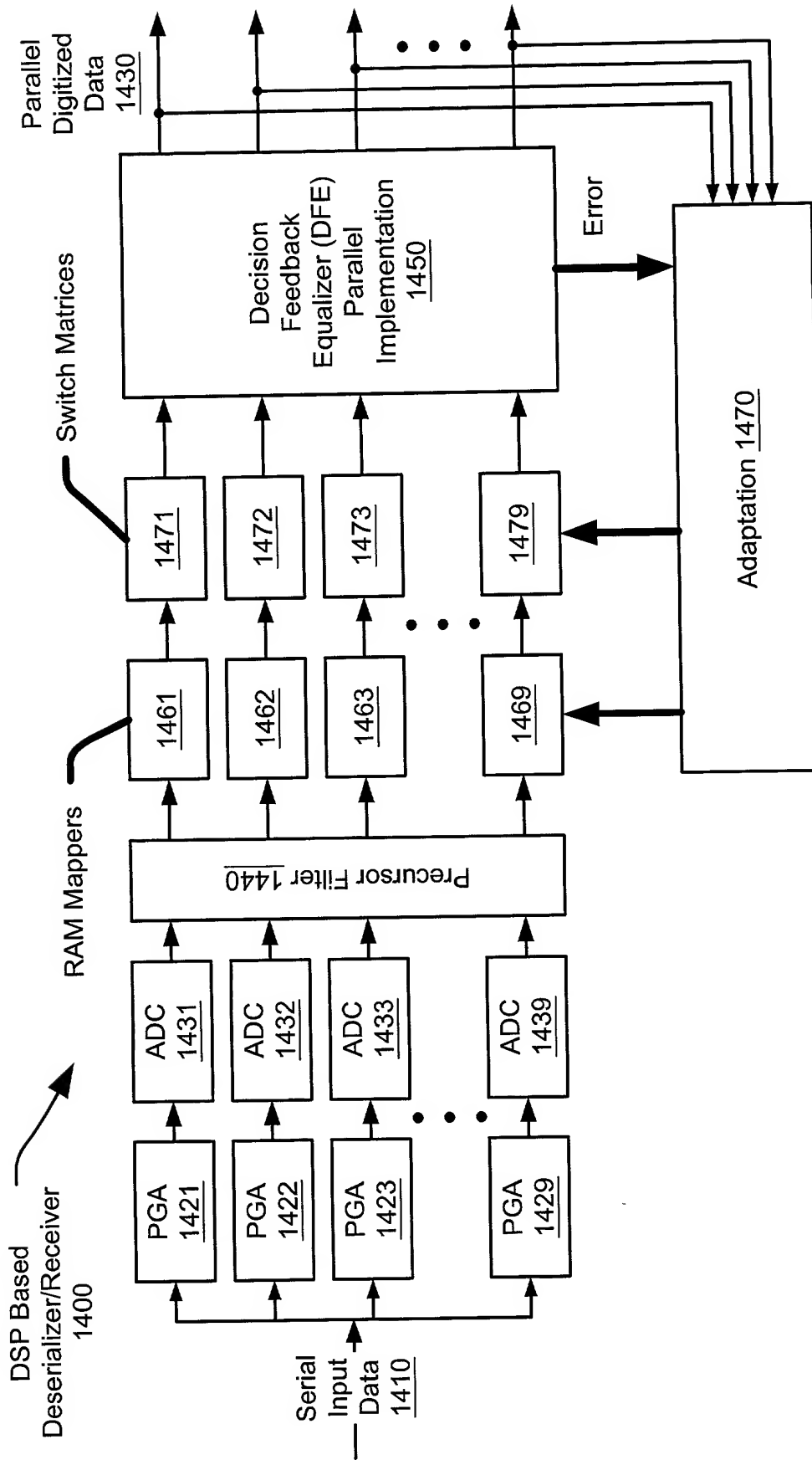


Fig. 14







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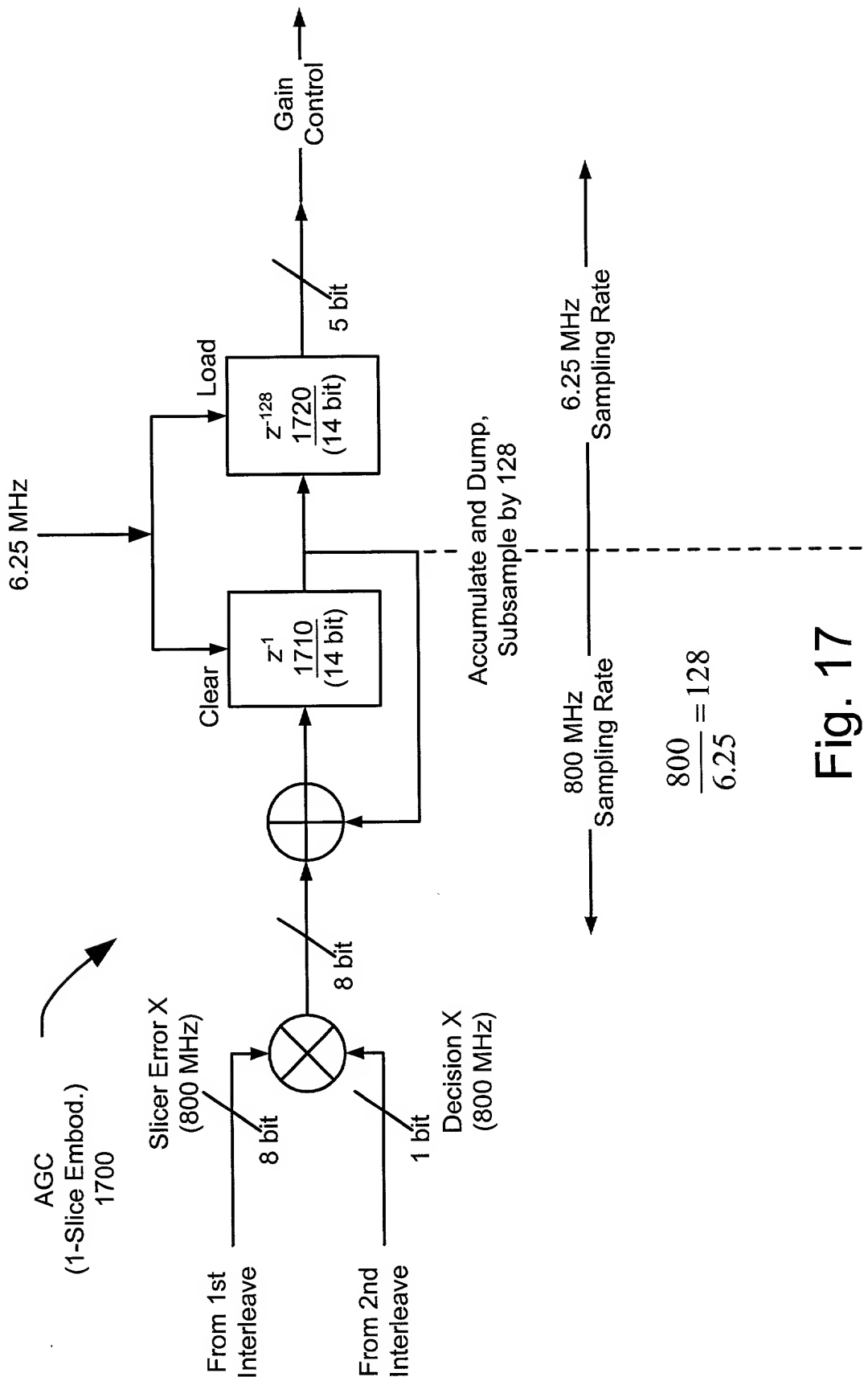


Fig. 17



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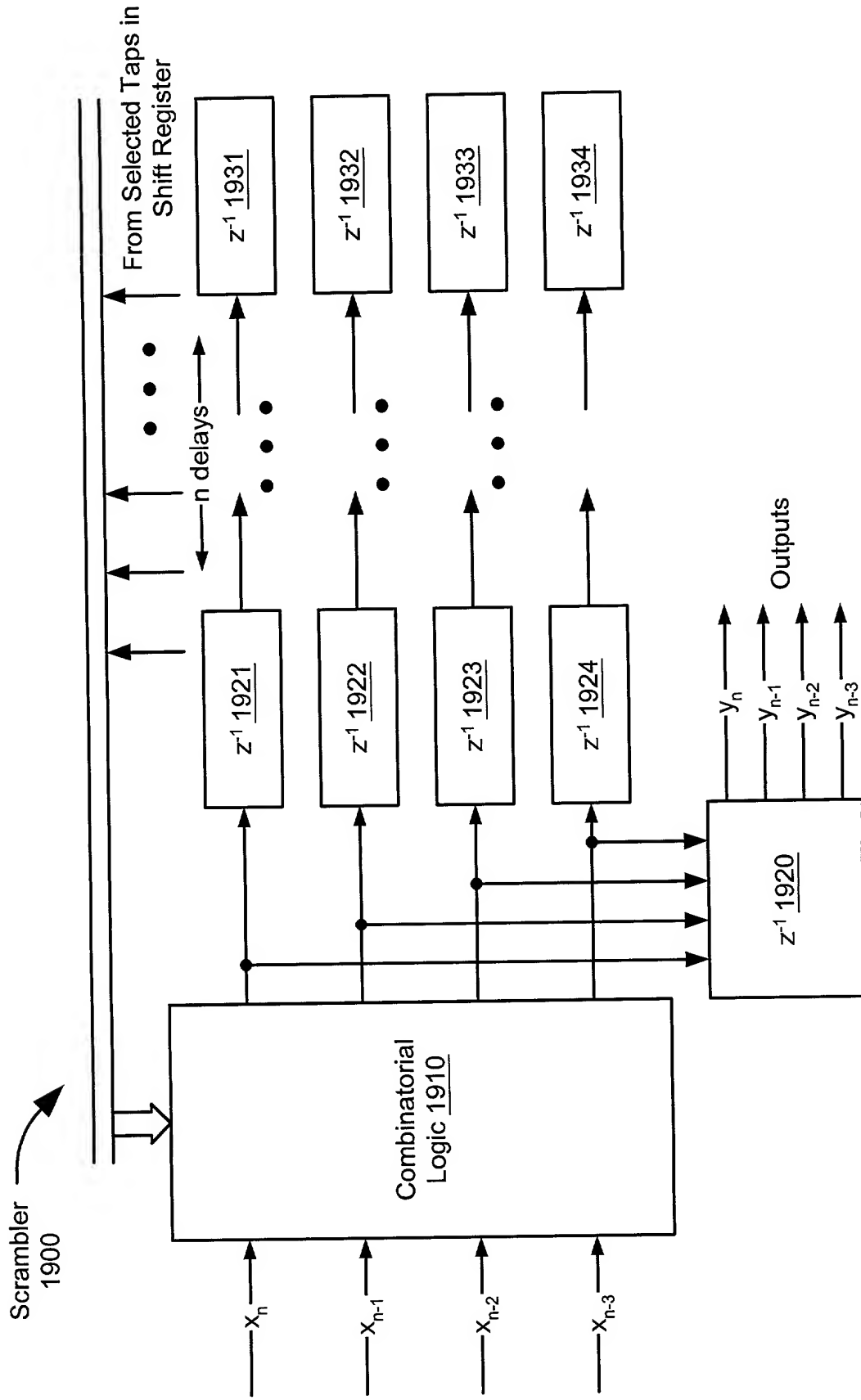


Fig. 19



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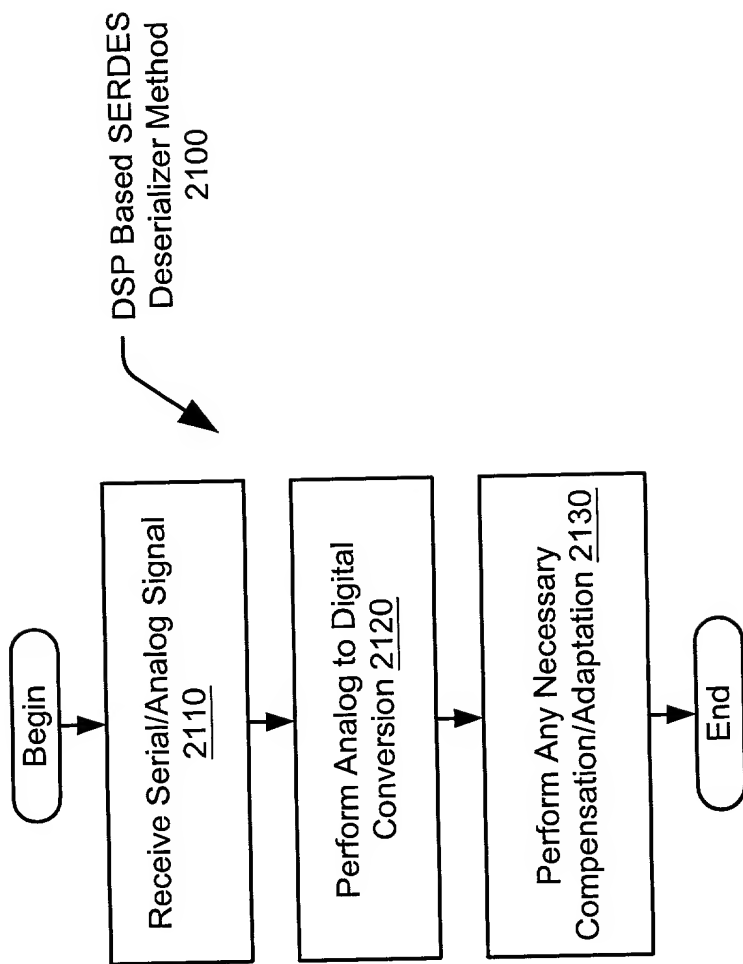


Fig. 21



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Begin

Receive Serial/Analog Signal 2310

Partition Serial/Analog Signal Using ADC Channel(s) 2320

DSP Based  
SERDES  
Deserializer  
Method 2300

Perform Any Necessary Compensation/Adaptation 2330

Before ADCs  
2332

After ADCs 2334

Jointly To All Devices 2340

All  
ADCs  
2341

All PGAs 2342

Using AGCs  
2343

Other Devices 2349

Individually To Devices 2350

ADC Basis  
2351

PGA Basis  
2352

Other Devices 2359

End

Fig. 23

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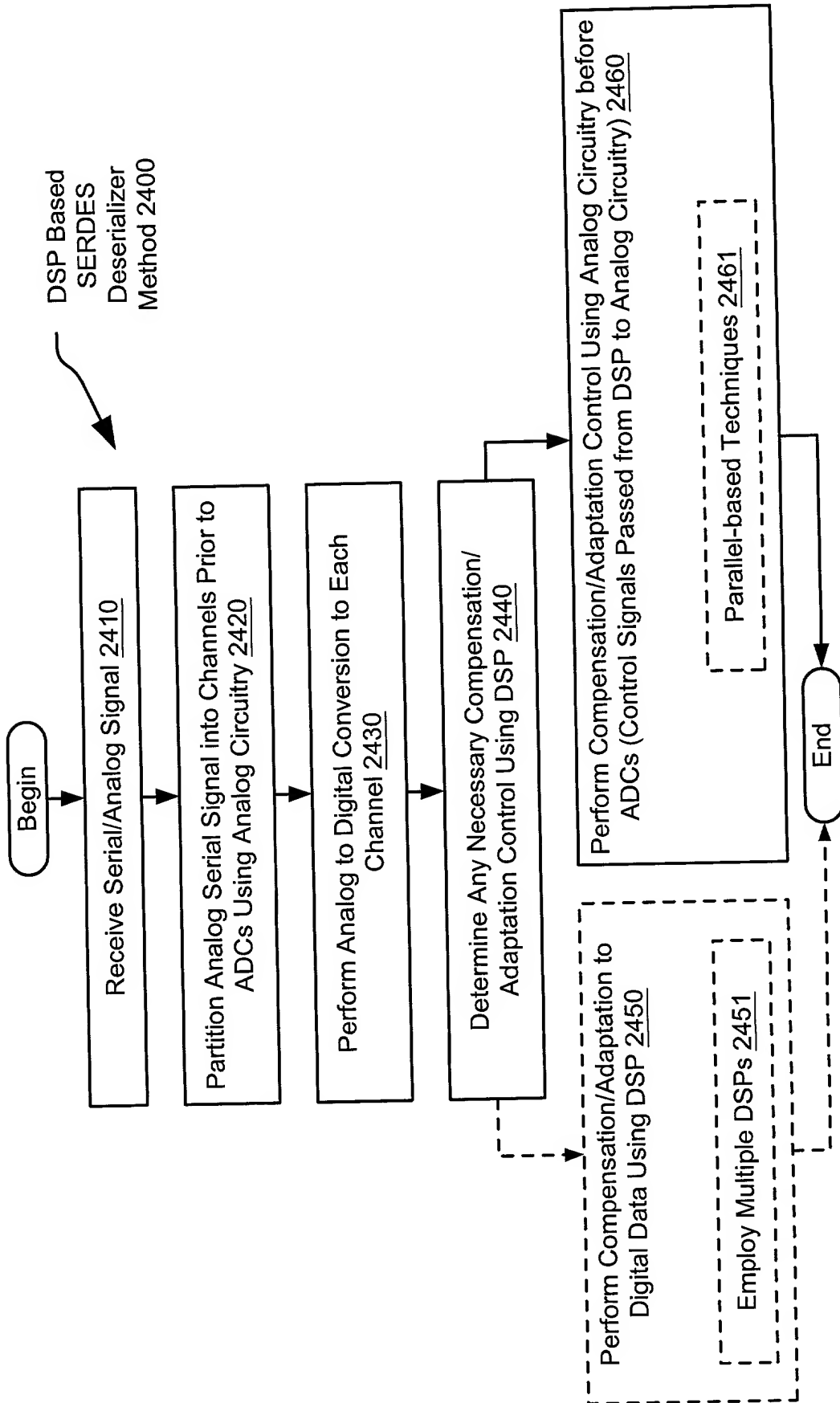


Fig. 24



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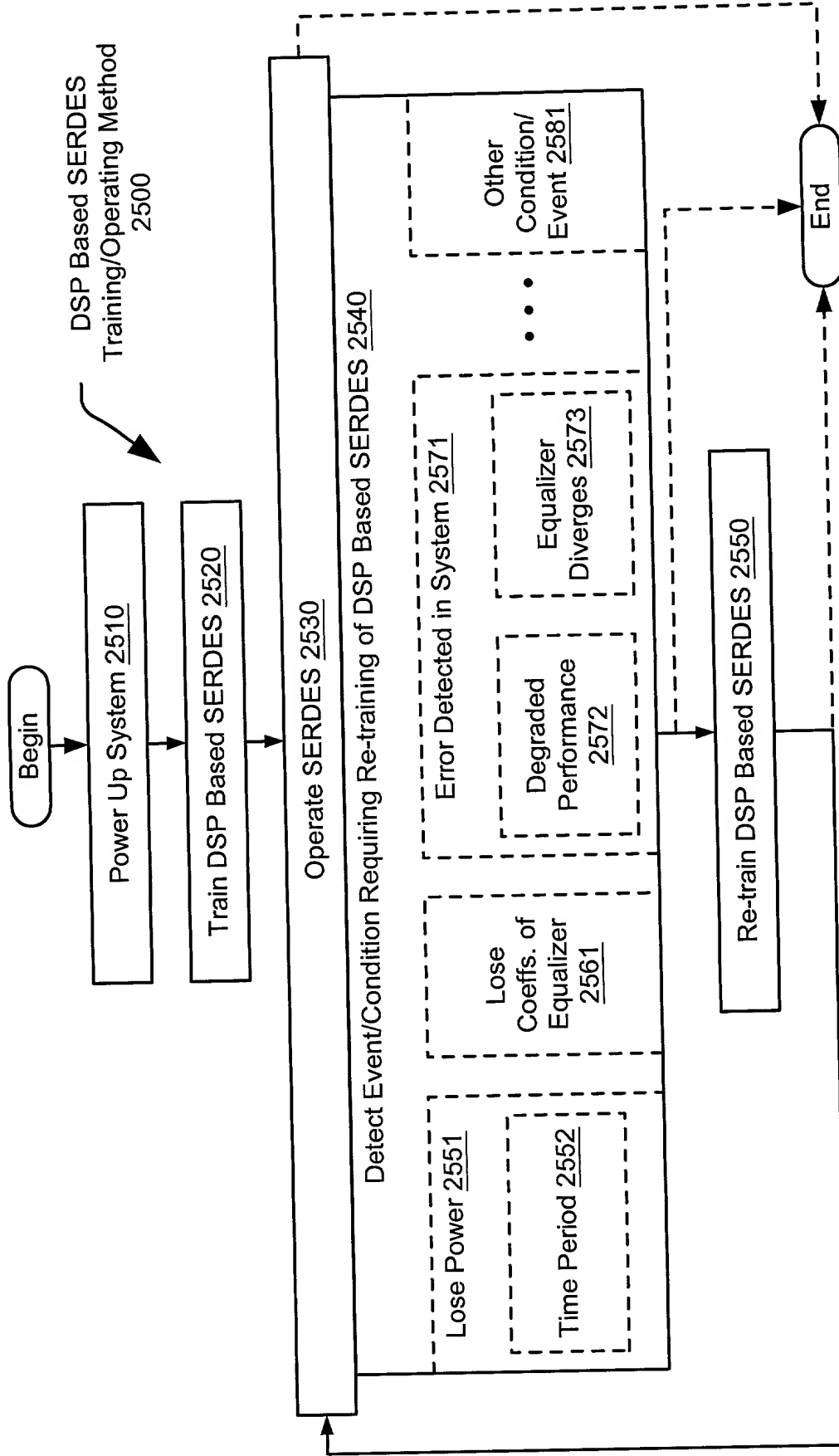


Fig. 25

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DSP Based SERDES Functionality 2600

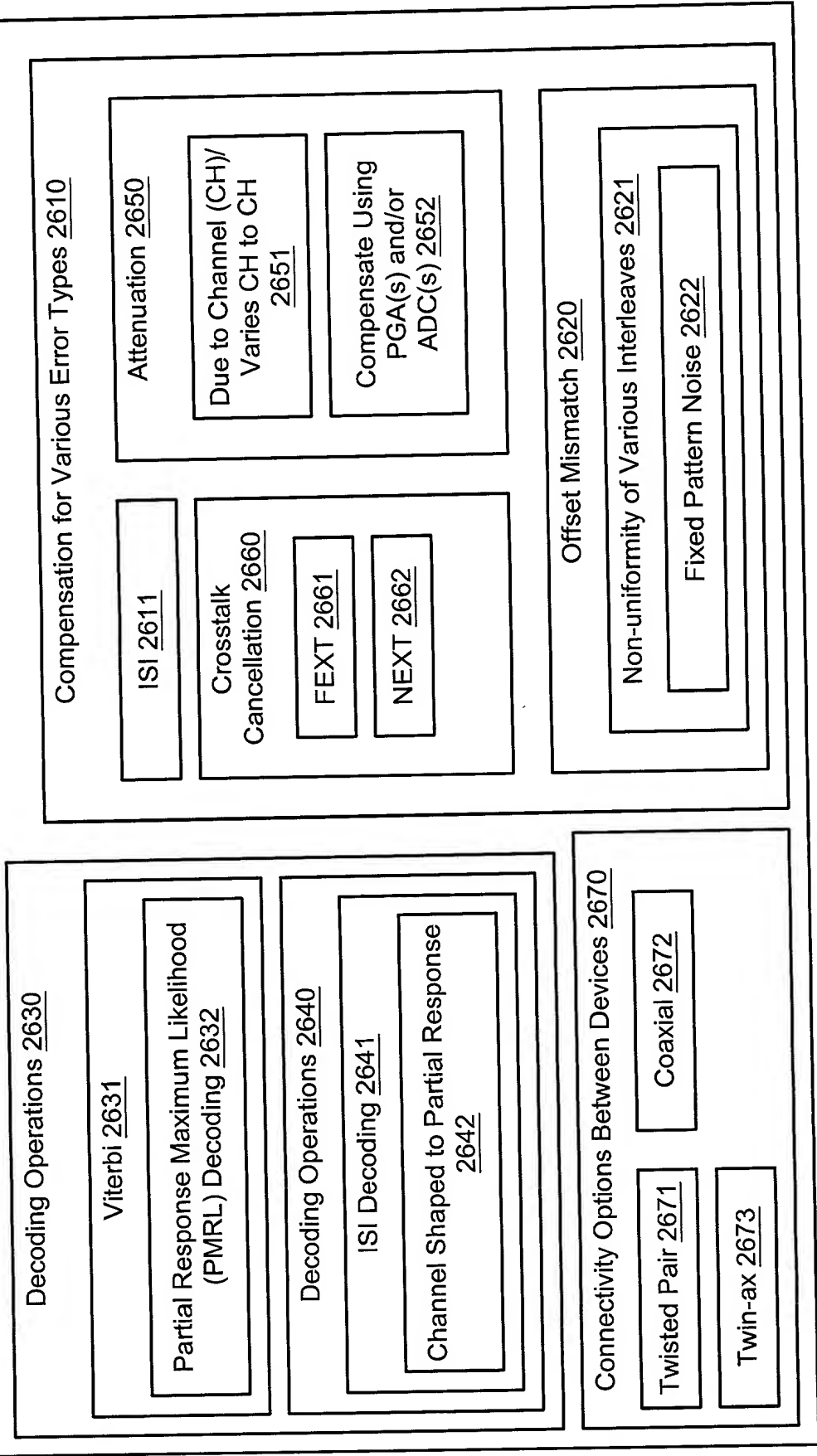


Fig. 26